FORM PTO-1390 (REV. 9-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **520.41005X00 filed Dec. 28, 2001**

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): **10/019406**

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/03476	June 29, 1999	

TITLE OF INVENTION: **SYSTEM LSI**

APPLICANT(S) FOR DO/EO/US: **SHIMURA, TAKANORI KOMATSU, KEIKO**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.

4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2)))
   a. ☐ is transmitted hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office(RO/US)

6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

14. ☐ A SECOND or SUBSEQUENT preliminary amendment.

15. ☐ A substitute specification.

16. ☒ A change of power of attorney and/or address letter.

17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.

18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).

19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).

20. ☒ Other items or information: **Figs. 1-11; PCT REQ. FORM; INT'L. SEARCH RPT.;INT'L. PRELIM. EXAM. RPT. IN THE ENGLISH AND JAPANESE LANGUAGES;INT'L. PUB. NO. WO01/01228; CREDIT CARD PAYMENT**

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/019406		520.41005X00

21. The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a) (1) - (5)):		
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1040.00		
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00		
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	- 20 =		x $18.00	$	
Independent Claims	- 3 =		x $84.00	$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$	
			TOTAL OF ABOVE CALCULATIONS =	$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$	
			SUBTOTAL =	$890.00	
Processing fee of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$	
			TOTAL NATIONAL FEE =	$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property			+	$40.00	
			TOTAL FEES ENCLOSED =	$930.00	
			Amount to be refunded:		$
			charged:		$

a. ☐ A check in the amount of $_____ to cover the fees is enclosed.

b. ☐ Please charge my Deposit Account No. **01-2135** in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposition Account No. **01-2135**. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Antonelli, Terry, Stout & Kraus, LLP
1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209
USA

SIGNATURE

Gregory E. Montone
NAME

28,141
REGISTRATION NO.

520.41005X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): SHIMURA et al.

Serial No.: Not yet assigned

Filed: On even date

For: SYSTEM LSI

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

December 28, 2001

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend claims 2, 4-9, 11-14 as follows:

2. (Amended) The semiconductor device according to claim 1, wherein said power-execution controlling means comprises;

means for storing information with regard to the power consumption, the individual bus operation time and a priority of data processing for respective operation modes of said plurality of functional units, and

means for assigning the power consumption and the individual bus operation time to the functional unit executing said processing successively from the functional units having higher priorities of data processing by using said information, setting the frequency of said clock signal in

correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

4. (Amended) The semiconductor device according to claim 1, wherein each of said plurality of functional units includes;

clock selecting means for selecting a clock signal having a corresponding frequency from the plurality of clock signals by receiving said clock control signal, and data processing means operating with the selected clock signal and setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal.

5. (Amended) The semiconductor device according to claim 1, wherein said power-execution controlling means includes means for detecting a change of the operation mode in said request of changing the operation mode and starts an operation of controlling the frequency of the clock signal and the bus operation time at a time point of detecting any change of the operation mode of the functional unit executing the processing.

6. (Amended) The semiconductor device according to any one of claim 1, wherein said power-execution controlling means includes means for calculating a total of the power consumption of the functional unit executing the processing and controls to lower the clock frequency of the functional unit having a low priority of data processing so that a total of the calculated power consumption does not exceed the limit of power consumption provided to the semiconductor device.

7. (Amended) The semiconductor device according to claim 1, further comprising:

voltage detecting means for detecting a voltage of a power source used internally,

wherein said power-execution controlling means calculates a total of the power consumption of the functional unit executing said processing by the voltage detected by using said voltage detecting means.

8. (Amended) The semiconductor device according to claim 1, further comprising:

an external memory for storing the information with regard to the power consumption, the individual bus operation time and the priority of data processing for respective operation modes of said plurality of functional units, and

external memory controlling means for controlling operation of the external memory,

wherein said power-execution controlling means comprises; storing means for storing the information of the external memory read by the external memory controlling means, and

means for assigning the power consumption and the individual bus operation time to the functional unit executing said processing successively from the functional units having higher priorities of data processing by using the information stored to said storing means, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

9. (Amended) The semiconductor device according to claim 1,

wherein each of said plurality of functional units includes sub memory means for storing the information with regard to the power consumption, the individual bus operation time and the priority of data processing for respective operation modes, and

wherein said power-execution controlling means includes;

storing means for reading and storing the information stored to the sub memory means, and

means for assigning the power consumption and the

individual bus operation time to the functional unit executing said processing successively from the functional units having higher priorities of data processing by using the information stored to the storing means, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

11. (Amended) The semiconductor device according to claim 10, wherein said power-execution control circuit comprises;

a power-execution control table for storing information with regard to the power consumption, the individual bus operation time and priorities of data processing for respective operation modes of said plurality of functional units,

a clock control circuit for assigning the power consumption to the functional unit executing said processing successively from the functional units having higher priorities of data processing by using said information and outputting said clock control signal by setting the frequency of the clock signal in correspondence with the assigned power consumption, and

a bus control circuit for assigning the individual bus operation time to the functional unit executing said processing successively from the functional units having the higher priorities of data processing and outputting said bus operation time control signal by setting the assigned individual bus operation time as said bus operation time.

12. (Amended) The semiconductor device according to claim 10, wherein said power-execution control circuit starts an operation of outputting said clock control signal and said bus operation time control signal at a time point of outputting a request of changing any operation mode of the functional unit executing the processing.

13. (Amended) The semiconductor device according to claim 10, wherein said power-execution control circuit includes a circuit for calculating a total of the power consumption of the functional unit executing the processing and controls to lower the clock frequency of the functional unit having a lower priority of data processing so that a total of the calculated power consumption does not exceed a limit of power consumption provided to the semiconductor device.

14. (Amended) The semiconductor device according to claim 10, further comprising:

a voltage detector for detecting a voltage of a power

source used internally,

wherein said power-execution control circuit calculates a total of the power consumption of the functional unit executing said processing by using the voltage detected by the voltage detector.

REMARKS

Entry of this amendment prior to examination is respectfully requested.

By the present amendment, the multiple dependent format of certain claims has been changed to single dependency format. Also, the term "block" used in claims 2, 8, 9 and 11 has been replaced with the term "unit" since this is the terminology used in the specification.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit

account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (520.41005X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

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Version with Markings to Show Changes Made

IN THE CLAIMS:

Claims 2, 4-9, 11 and 14 have been amended as follows:

2. (Amended) The semiconductor device according to claim 1, wherein said power-execution controlling means comprises;

means for storing information with regard to the power consumption, the individual bus operation time and a priority of data processing for respective operation modes of said plurality of functional units, and

means for assigning the power consumption and the individual bus operation time to the functional [block] unit executing said processing successively from the functional [blocks] units having higher priorities of data processing by using said information, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

4. (Amended) The semiconductor device according to [any one of claims 1 through 3] claim 1, wherein each of said plurality

of functional units includes;

clock selecting means for selecting a clock signal having a corresponding frequency from the plurality of clock signals by receiving said clock control signal, and data processing means operating with the selected clock signal and setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal.

5. (Amended) The semiconductor device according to [any one of claims 1 through 3] claim 1, wherein said power-execution controlling means includes means for detecting a change of the operation mode in said request of changing the operation mode and starts an operation of controlling the frequency of the clock signal and the bus operation time at a time point of detecting any change of the operation mode of the functional unit executing the processing.

6. (Amended) The semiconductor device according to any one of [claims 1 through 3] claim 1, wherein said power-execution controlling means includes means for calculating a total of the power consumption of the functional unit executing the processing and controls to lower the clock frequency of the functional unit having a low priority of data processing so that a total of the calculated power consumption does not exceed the limit of power consumption provided to the semiconductor device.

7. (Amended) The semiconductor device according to [any one of claims 1 through 3] claim 1, further comprising:

voltage detecting means for detecting a voltage of a power source used internally,

wherein said power-execution controlling means calculates a total of the power consumption of the functional unit executing said processing by the voltage detected by using said voltage detecting means.

8. (Amended) The semiconductor device according to claim 1, further comprising:

an external memory for storing the information with regard to the power consumption, the individual bus operation time and the priority of data processing for respective operation modes of said plurality of functional units, and

external memory controlling means for controlling operation of the external memory,

wherein said power-execution controlling means comprises; storing means for storing the information of the external memory read by the external memory controlling means, and

means for assigning the power consumption and the individual bus operation time to the functional [block] unit executing said processing successively from the functional [blocks] units having higher priorities of data processing by using the information stored to said storing means, setting

the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

9. (Amended) The semiconductor device according to claim 1,

wherein each of said plurality of functional units includes sub memory means for storing the information with regard to the power consumption, the individual bus operation time and the priority of data processing for respective operation modes, and

wherein said power-execution controlling means includes;

storing means for reading and storing the information stored to the sub memory means, and

means for assigning the power consumption and the individual bus operation time to the functional [block] unit executing said processing successively from the functional [blocks] units having higher priorities of data processing by using the information stored to the storing means, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set

frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

11. (Amended) The semiconductor device according to claim 10, wherein said power-execution control circuit comprises;

a power-execution control table for storing information with regard to the power consumption, the individual bus operation time and priorities of data processing for respective operation modes of said plurality of functional units,

a clock control circuit for assigning the power consumption to the functional [block] unit executing said processing successively from the functional [blocks] units having higher priorities of data processing by using said information and outputting said clock control signal by setting the frequency of the clock signal in correspondence with the assigned power consumption, and

a bus control circuit for assigning the individual bus operation time to the functional [block] unit executing said processing successively from the functional [blocks] units having the higher priorities of data processing and outputting said bus operation time control signal by setting the assigned individual bus operation time as said bus operation time.

12. (Amended) The semiconductor device according to claim 10

[or 11], wherein said power-execution control circuit starts an operation of outputting said clock control signal and said bus operation time control signal at a time point of outputting a request of changing any operation mode of the functional unit executing the processing.

13. (Amended) The semiconductor device according to claim 10 [or 11], wherein said power-execution control circuit includes a circuit for calculating a total of the power consumption of the functional unit executing the processing and controls to lower the clock frequency of the functional unit having a lower priority of data processing so that a total of the calculated power consumption does not exceed a limit of power consumption provided to the semiconductor device.

14. (Amended) The semiconductor device according to claim 10 [or 11], further comprising:

a voltage detector for detecting a voltage of a power source used internally,

wherein said power-execution control circuit calculates a total of the power consumption of the functional unit executing said processing by using the voltage detected by the voltage detector.

DESCRIPTION

SYSTEM LSI

Technical Field

The present invention relates to a system on chip technology for integrating a circuit having a system function in a single piece of chip, particularly to a semiconductor device constituted by a plurality of functional units for executing a plurality of kinds of data processing by using the functional units.

Background Art

A system LSI (Large Scale Integrated circuit) is mounted with a plurality of functional units and executes various kinds of data processing by connecting these by a bus (common line). According to such a system LSI, it is normal that an integration scale is generally large and power consumption is increased in accordance therewith. Therefore, a chip is set with a limit of power consumption determined by a package, a cooling condition or the like. For example, according to a normal plastic package, an upper limit value thereof is about 1.5 watt. When the value is exceeded, operation temperature of the chip is elevated and LSI is operated erroneously. Therefore, conventionally, a total of maximum power consumption probable in all of the

functional units is defined as power consumption of the system LSI and LSI is designed so that the power consumption does not exceed a limit of the power consumption.

Further, there also is carried out a design for reducing power consumption of a system LSI switched ON with a power source within a range of the limit of power consumption. A number of the system LSI is constituted by a CMOS (Complementary Metal Oxide Semiconductor) circuit and therefore, when a clock frequency is lowered, power consumption of the CMOS circuit is reduced. Hence, there has been carried out a control of reducing a frequency of a clock signal to a functional unit which is not related to specific operation, that is, a functional unit which does not execute data processing or stopping a clock therefor. Each functional unit is operated in accordance with instruction of CPU and therefore, there is carried out such a control of low power consumption formation to a functional unit which needs not to execute the instruction. For example, Japanese Patent Laid-Open (Kokai) No. Hei 8-272479, describes that power consumption is reduced by increasing a clock frequency of a functional unit executing instruction of CPU and reducing a clock frequency of a functional unit which does not need to execute the CPU instruction.

In recent years, progress of the multimedia field is remarkable and in accordance therewith, there is increased market needs for a system LCI integrated with a microprocessor

having both of high function and low power consumption performance and exclusive functional units.

Further, by progress of technology of fabricating a semiconductor, a number of gates which can be integrated, exceeds a million gates and a number of functional units are integrated to the same chip. Therefore, even when power consumption of each functional unit is small, power consumption is increased by simultaneously operating all the integrated functional units and it becomes difficult to design LSI so that a total of maxima of power consumption of all the functional units does not exceed the limit of power consumption of LSI.

Therefore, in order to increase the limit of power consumption, adoption of an expensive package having a heat radiating effect or forced cooling such as air cooling or water cooling is unavoidable and there is brought about a situation in which low cost forming means such as use of an inexpensive package or under a windless state cannot be used.

Disclosure of Invention

It is an object of the invention to provide a semiconductor device capable of mounting a number of functional units without using a package having a high heat radiating effect or forced cooling.

There is normally included a functional unit capable of reducing operation frequency in comparison with other

functional unit in a plurality of functional units mounted to a system LSI in executing instruction of CPU. For example, in a system LSI used in a digital TV in the multimedia field, a game machine or the like, there are integrated various kinds of functional units such as graphics, image processing, voice processing, peripheral interface or the like, among them, graphics, peripheral interfaces or the like are frequently permitted to reduce operation frequency. Meanwhile, in cases of image processing and voice processing, real time processings are frequently executed and therefore, set operation frequencies are frequently not permitted to change.

Further, operation frequency of a functional unit is set in accordance with content of data processing. For example, in the case of image processing, there is set operation frequency which differs in accordance with resolution of image to be processed or degree of image compression.

Further, in the following, assume that a state of operating at a certain frequency is referred to as an operation mode at the frequency. For example, when there are high frequency, middle frequency and low frequency in the frequency and a functional unit is operated at middle frequency, the functional unit is brought into an operation mode of middle frequency.

The inventors have paid attention to the fact that even when a total of maximum power consumption probable in all the functional units exceeds the limit of power consumption,

operation can be carried out when a total of instantaneous power consumption (hereinafter, the total is referred to as "peak power consumption") of functional units in operation, does not exceed the limit of power consumption and such a peak power consumption can be set by controlling operation frequency for each of the functional units executing the processing. In such a case, a priority is set in accordance with a degree of probability of changing operation frequency in accordance with content of the processing. That is, when the operation frequency cannot be changed, the priority becomes higher and when the operation frequency can be changed, the priority becomes lower.

The invention has been carried out in view of the above-described. That is, in order to achieve the above-described object, according to the invention, there is provided a semiconductor device characterized in comprising operation mode outputting means provided to each of a plurality of functional units for outputting a request of changing an operation mode at a frequency in operation to other operation mode in accordance with a data processing content, and power-execution controlling means for controlling a frequency of a clock signal and a bus operation time used by the functional unit executing a processing so that a total of power consumption of the functional unit executing the processing in the plurality of functional units does not exceed limit of power consumption

provided to the semiconductor device in accordance with the request of changing the operation mode.

When such means are adopted, the functional units are operated by operation modes in accordance with a processing content of a real time processing or the like and accordingly, a number of the functional units can be operated by power consumption lower than maximum power consumption thereof and there can be realized the semiconductor device capable of mounting a number of functional units without using a package having a high heat radiating effect or forced cooling.

The power-execution controlling means can be constituted by, for example, means for storing information with regard to the power consumption, the individual bus operation time and a priority of data processing for respective operational modes of the plurality of functional units and means for assigning the power consumption and the individual bus operation time to the functional block executing the processing successively from the functional blocks having higher priorities of data processing by using the information, setting the frequency of the clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as the bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing

the processing.

Further, the means for storing the information can be constituted by a power-execution control table for storing the information, and the means for supplying the clock control signal and the bus operation time control signal to the functional unit executing the processing, can be constituted by a clock control circuit and a bus control circuit respectively generating and outputting the clock control signal and the bus operation time control signal.

Each of the plurality of functional units can further be constituted by clock selecting means for selecting a clock signal having a corresponding frequency from the plurality of clock signals by receiving the clock control signal, and data processing means operated by the selected clock signal and setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal in addition to the operation mode outputting means.

Further, although in the above-described, the storing means of the power-execution controlling means stores the information of the respective functional units together, separately therefrom, it is possible that the information of the respective functional units is stored to a memory apparatus (memory) at outside of the semiconductor device, the power-execution control means reads the information stored to the external memory apparatus in initializing and stores the

information to the storing means and the clock frequency and the bus operation time of the functional unit executing the processing are controlled by using the stored information.

That is, the power-execution control means assigns the power consumption and the individual bus operation time to the functional block executing the processing by using the information stored to the storing means successively from the functional blocks having higher priorities of data processing, sets the frequency of the clock signal in correspondence with the assigned power consumption and sets the assigned individual bus operation time as the bus operation time, and supplies the clock control signal for causing to operate at the set frequency of the clock signal and the bus operation time control signal for causing to use the set bus operation time to the functional unit executing the processing.

Further, further separately therefrom, it is possible that each of the functional units includes sub memory means, the information of the functional unit per se is stored to the sub memory means and the power-execution control means reads the respective information stored to the sub memory means in initializing and stores the information together to the storing means and controls the clock frequency and the bus operation time of the functional unit executing the processing by using the stored information.

That is, the power-execution control means assigns the

power consumption and the individual bus operating time to the functional block executing the processing by using the information stored to the storing means successively from the functional blocks having higher priorities of data processing, sets the frequency of the clock signal in correspondence with the assigned power consumption and sets the assigned individual bus operation time as the bus operation time, and supplies the clock control signal for causing to operate at the set frequency of the clock signal and the bus operation time control signal for causing to use the set bus operating time to the functional unit executing the processing.

Brief Description of Drawings

Fig. 1 is a block diagram of a system LSI for explaining a first embodiment of a semiconductor device according to the invention, Fig. 2 is a block diagram of a clock selector used in the first embodiment, Fig. 3 is a diagram for explaining information stored in a power-execution control table used in the first embodiment, Fig. 4 is a diagram for explaining a sequence of power consumption and bus operation time control in the first embodiment, Fig. 5 is a flowchart diagram for explaining the power consumption control in the first embodiment, Fig. 6 is a flowchart diagram for explaining the bus operation time control in the first embodiment, Fig. 7 is a block diagram for explaining a bus control circuit used in the first embodiment,

Fig. 8 is a circuit diagram for explaining a voltage detector used in the first embodiment, Fig. 9 is a block diagram of a system LSI for explaining a second embodiment of the invention, Fig. 10 is a block diagram of a system LSI for explaining a third embodiment of the invention, and Fig. ~~11~~ is a diagram for explaining information stored to a power-execution memory of a functional unit used in the third embodiment.

Best Mode for Carrying Out the Invention

Further detailed explanation will be given of a semiconductor device according to the invention in reference to several embodiments illustrated in the drawings as follows. Further, the same notation in Fig. 1 through Fig. 11 indicates the same object or a similar object.

(Embodiment 1)

Fig. 1 is a block diagram of a system LSI showing a first embodiment of the invention. The system LSI is constituted by a clock generator 101, functional units 104 through 107, a power-execution control circuit 109 and a voltage detector 110. Specifically, the functional unit 104 is a microprocessor, the functional unit 105 is an image processing circuit, the functional unit 106 is a voice processing circuit and the functional unit 107 is a peripheral module. The functional units 104 through 107, the power-execution control circuit 109 and the voltage detector 110 are connected to each other by

an internal bus 10.

The clock generator 101 is constituted by a clock oscillator 102 and a clock divider 103 for subjecting an output signal of the clock oscillator 102 to frequency conversion into clock signals 115a through 115c from high frequency to low frequency by the clock divider 103 and distributing the clock signals to the functional units 104 through 107. Frequencies of clock used in the embodiment are three kinds of high frequency, middle frequency and low frequency.

The functional units 104 through 107 are respectively constituted by clock selectors 214 through 217, data processing circuits 224 through 227 and operation mode output circuits 304 through 307.

The clock selectors 214 through 217 select predetermined clocks from the plurality of input clocks 115a through 115c in accordance with clock control signals 414 through 417 from the power-execution control circuit 109.

The data processing circuits 224 through 227 execute operation processing or data processing necessary in the functional units. Operation processing frequency at this occasion is dependent on clock frequencies selected by the clock selectors 214 through 217. When high-speed clock is selected, operation is executed at high frequency and when low frequency clock is selected, operation is executed at low frequency.

When operation modes at frequencies designated by the

clock control signals 414 through 417 are incosistent with operation modes necessary in view of contents of processings, the operation mode output circuits 304 through 307 output operation mode change request signals requesting in which operation modes (high frequency, middle frequency, low frequency) the functional units 104 through 107 intend to operate, to the power-execution control circuit 109 as operation mode output signals 444 through 447.

The power-execution control circuit 109 is constituted by a power-execution control table 404 constituting storing means, a clock control circuit 401 and a bus control circuit 402 and control operation clock frequency and bus operation time in correspondence with the operation mode change request signals 444 through 447 outputted from the respective functional units.

The power-execution control table 404 is stored with information with regard to power consumption, individual bus operation time and priority of processing in accordance with operation mode of each functional unit.

The clock control circuit 401 controls operation clock frequency of each functional unit so that a functional unit having a high priority of processing is acknowledged to consume more power and with regard to a functional unit having a low priority, consumed power is reduced in reference to the operation mode change request signals 444 through 447 outputted from the

respective functional units and power consumption and priority of the power-execution control table 404.

The bus control circuit 402 gives more bus operation time to a unit having a high priority of processing and controls bus operation time with regard to a functional unit having a low priority so that bus operation time is shortened in reference to individual bus operation time of the power-execution table 404 and operation clock frequency (operation mode) of each functional unit determined by the clock control circuit 401 to thereby control bus transfer speed.

The voltage detector 110 is a circuit for calculating actual operation voltage of LSI by comparing reference voltage Vref supplied from outside of LSI and power source voltage of LSI.

An explanation will be given of operation of the respective circuits as follows. The functional units 104 through 107 are operated by a clock at low frequency having small power consumption, that is, brought into an operation mode at low frequency at an initial state of operation. When following factors are present, each functional unit changes the operation mode in correspondence with the factors to thereby meet processing request. The factors for changing the operation mode in the respective functional unit are as follows.

In the case of the microprocessor 104, the microprocessor 104 is changed into an operation mode which needs high frequency

processing by an interruption request (604) such as keyboard, peripheral device or the like from outside. Further, also when a processing program which needs high frequency or middle frequency processing in the microprocessor 104, the microprocessor 104 is changed into an operation mode which needs high frequency or middle frequency processing.

According to the image processing circuit 105, the operation mode is changed by setting parameters of image processing such as image quality, pixel size, frame number, encoding system or the like from the microprocessor 104. When an image having a high image quality is processed, high frequency processing is requested. Further, when a processing is executed by thinning a frame or a field or coarsening image quality, image processing can be executed at comparatively low frequency.

In the case of the voice processing circuit 106, processing frequency differs by sound quality or encoding system. When voice having high quality is encoded or decoded, the voice processing circuit is changed into high-speed operation mode. Further, in the case of voice processing, there is a case in which a real time processing is indispensable and in order to realize the real time processing, it is necessary to heighten a priority of processing and execute the processing more predominantly than other functional units.

In the case of the peripheral module 107, operation mode is changed by data transfer request (607) from peripheral device

or a network or an amount of data transmitted per unit time. When the amount of data is large, high speed processing is needed and when the data amount is small or a network is retarded, these can be dealt with sufficiently by low frequency processing.

When the functional units 104 through 107 receive these request signals at inside thereof, the functional units output the operation mode change requests 444 through 447 from the operation mode output circuits 304 through 307 to the power-execution control circuit 109.

In correspondence with the operation mode change requests 444 through 447 from the respective functional units, the power-execution control circuit 109 heightens a frequency of an operation clock of each functional unit and changes allocation of the bus operation time to prolong in accordance with the priority of processing of each functional unit.

Further, the power-execution control circuit 109 lowers the frequency of the operation clock of each functional unit and changes allocation of the bus operation time to shorten when each functional unit transmits a request to change to a mode operating at low frequency after temporarily constituting operation mode at high frequency.

Fig. 2 shows a constitution of the clock selector 214. In the drawing, there are also shown waveforms of three kinds of the clock signals 115a through 115c. Relative to a clock frequency fc, a frequency of the high speed clock signal 115a

is 2fc twice as much as the clock frequency fc and a frequency of the low frequency clock signal 115a is fc/2 of a half thereof. The clock selector 214 is constituted by a selector 234 of clock and switches the three kinds of clocks 115a through 115c by using the clock control signal 414.

The clock switch control signal 414 is a signal of 2 bits, and with regard to 2 bits, frequencies are set as follows.

(0,0): Middle frequency clock (115b)

(0,1): Low frequency clock (115c)

(1,0): High frequency clock (115a)

(1,1): Prohibition (clock signal is not selected)

Further, although according to the example, the multiplication factor is set to twice and half, clock radio is not specified thereto.

Further, although according to the invention, an explanation has been given such that the clock divider 103 is arranged at inside of the clock selector 101, clock can be controlled to switch by arranging the clock divider 103 to inside of each of the clock selectors 214 through 217.

Next, an explanation will be given of the power-execution control circuit 109. First, an explanation will be given of data set to the power-execution control table 404. Fig. 3 shows an example of data stored to the power-execution speed control table 404.

There are three kinds of a high frequency clock mode (200 MHz),

a middle frequency clock mode (100 MHz) and a low frequency clock mode (50 MHz) in the operation modes and power consumption 451a, individual bus operation time 451b and priority of data processing 451c are stored for respective mode. Although according to the example, the high frequency clock mode is set to 200 MHz, the middle frequency clock mode is set to 100 MHz and the low frequency clock mode is set to 50 MHz, operation clock frequencies are not specified to these.

The power consumption 451a exemplifies maximum power consumption at each operation clock mode.

The bus operation time 451b registers time used in unit time controlling the bus in % display. For example, when the unit time is 10 microseconds, 20 % indicates that time of 2 microseconds is used for each 10 microseconds.

The priority of data processing 451c is indicated by 10 stages from 1 to 10 in this example. Numeral 1 indicates the highest priority and numeral 10 indicates the lowest setting. When operation mode change requests are simultaneously outputted from a plurality of functional units, power consumption and bus operation time are assigned successively from functional units having higher priorities of data processing.

Functional units having lower priorities, are assigned with power consumption and bus operation time respectively from remaining power consumption produced by subtracting power

consumption used in functional units having higher priorities from total power consumption and remaining bus operation time produced by subtracting bus operation time used by functional units having higher priorities from total bus operation time and are operated by operation modes (low operation clock frequencies) operated in the power consumption and the bus operation time.

Next, an explanation will be given of a way of determining the priority of data processing. The more the real time processing is needed, the higher the priority is set. As conditions necessary for executing the real time processing, there are processing frequency and bus transfer speed (here, assigned to each functional unit as bus operation time). In executing the real time processing, both factors are taken into consideration.

For example, in image processing, it is necessary to set both of the operation frequency and bus transfer speed. In network control, although the operation frequency is not needed, the data transfer speed is frequently needed. Further, with regard to voice processing, real time data transfer without delay is needed.

According to the embodiment, the priority of data processing is made to differ for respective operation mode. Therefore, for example, when both of the microprocessor 104 and the image processing circuit 105 are operated at high

frequency operation mode (200 MHz), the priority of the image processing circuit 105 becomes higher, however, when the microprocessor 104 is brought into high frequency operation mode (200 MHz) and the image processing circuit is brought into middle frequency operation mode (100 MHz), the priority of the microprocessor 104 becomes higher. In this way, the priority can also be controlled to reverse by the operation mode.

Although according to the embodiment, an explanation has been given by indicating the priority of data processing by 10 stages, a method of setting the priority is not specified thereto. For example, the priority may be assigned by 8 bits and in this case, the priority can be selected from 256 priorities.

Next, an explanation will be given of a sequence of power consumption control and bus operation time control executed in the embodiment. The operation mode output signals 444 through 447 are signals of 2 bits and a content of request is set as follows.

(0, 0): Middle frequency operation mode request

(0, 1): Low frequency operation mode request

(1, 0): High frequency operation mode request

(1, 1): Prohibition

Assume that in Fig. 4, at time T0, the microprocessor 104, the image processing circuit 105 and the peripheral module 107 are operated by low frequency operation mode and the voice

processing circuit 106 is operated at high frequency operation mode.

Assume that at time T1, the data transfer request 607 is inputted from a peripheral bus to the peripheral module 107. In accordance with the request, the peripheral module 107 outputs the request 447 for changing from low frequency operation mode to high frequency operation mode, to the power-execution control circuit 109.

The power-execution control circuit 109 receives the operation mode change request 447. The clock control circuit 401 is provided with a circuit of detecting reception of the operation mode change requests 444 through 447 and upon detecting the reception, the clock control circuit 401 starts operating to immediately generate a clock control signal. Upon receiving the operation mode change request 447, the clock control circuit 401 reads power consumption (0.15 W) and the priority of data processing (10) of the microprocessor 104 in low frequency operation mode, power consumption (0.15 W) and the priority of processing (8) of the image processing circuit 105 in low frequency operation mode, power consumption (0.4 W) and the priority of data processing (1) of the voice processing circuit 106 in high frequency operation mode and power consumption (0.2 W) and the priority of data processing (3) of the peripheral module 107 in high frequency operation mode, stored in the power-execution control table (refer to Fig. 3), and calculates

power consumption assigned to the respective functional units in accordance with a flowchart diagram of Fig. 5. A detailed explanation will be given separately to the flowchart of Fig. 5.

Here, a total (0.9 W) of power consumption of the four functional units 107 through 107 does not exceed a limit of power consumption (1.5 W) and therefore, in accordance with the request of changing the operation mode of the peripheral module 107, the operation mode (clock frequency) of the peripheral module 107 is changed to high frequency mode.

Next, in accordance with the operation mode determined by the clock control circuit 401, the bus control circuit 402 reads bus operation time (5 %) and the priority of data processing (10) of the microprocessor 104 in low frequency operation mode, bus operation time (12 %) and the priority of data processing (8) of the image processing circuit 105 in low frequency operation mode, bus operation time (5 %) and the priority of data processing (1) of the voice processing circuit 106 in high frequency operation mode and bus operation time (40 %) and the priority of data processing (3) of the peripheral module (107) in high frequency operation mode, stored in the power-execution table 404 (refer to Fig. 3), and calculates bus operation time assigned to the respective functional units in accordance with a flowchart diagram of Fig. 6. With regard to the flowchart of Fig. 6, a detailed explanation will be given separately.

Here, a total (62 %) of the bus operation time of the four functional units 104 through 107 does not exceed 100 % and therefore, the bus operation time necessary for all the functional units can be assigned.

Successively, assume that at time T2 (Fig. 4), an interruption 604 is inputted to the microprocessor 104 and the microprocessor 104 outputs the change request 444 from low frequency operation mode to high frequency operation mode. Similar to the case of time T1, the power-execution control circuit 109 determines operation modes (operation clocks) of the microprocessor 104 and the other functional units from power consumption and priorities of data processing in correspondence with operation modes of the respective functional units. Further, bus operation time of the microprocessor 104 and the other functional units is determined from bus operation time and priorities of data processing in correspondence with the operation modes of the respective functional units. Also in this case, similar to time T1, a total of power consumption (1.35 W = 0.6 W +0.15 W + 0.4 W + 0.2 W) is equal to or smaller than the limit of power consumption, a total (77 % = 20 % + 12 % + 5 % + 40 %) of bus operation time does not reach 100 % and therefore, the microprocessor 104 transits to high frequency operation mode and power consumption of the microprocessor 104 becomes 0.6 W and the bus operation time becomes 20 %.

Assume that at time T3, the image processing circuit 105

is designated to promote quality of image from the microprocessor 104 and the image processing circuit 105 outputs the request 445 of changing from low frequency operation mode to high frequency operation mode. Similar to the cases of time T1 and time T2, the power-execution control circuit 109 determines operation modes (operation clocks) of the image processing circuit 105 and the other functional units from power consumption and priorities of data processings in correspondence with operation modes of the respective functional units. Further, bus operation time of the image processing circuit 105 and the other functional units is determined from individual bus operation time and priorities of data processings in correspondence with the operation modes of the respective functional units.

Assuming that the image processing circuit 105 is changed to high frequency operation mode, a total of power consumption becomes 1.8 W to exceed the limit of power consumption by adding 0.6 W of the microprocessor 104 operated in high frequency operation mode, 0.6 W of the image processing circuit 105 assumed to operate in high frequency operation mode, 0.4 W of the processing circuit 106 operated in high frequency operation mode and 0.2 W of the peripheral module 107 operated in high frequency operation mode.

Hence, power consumption of a functional unit having a low priority is controlled to reduce. All of the four functional

units are assumed to operate in high frequency operation mode and therefore, the priority of the microprocessor 104 is 4, the priority of the image processing circuit 2, the priority of the voice processing circuit 106 is 1 and the priority of the peripheral module 107 is 3 and therefore, the operational mode of the microprocessor 104 having the lowest order of the priority is lowered from high frequency to middle frequency. As a result, power consumption of the microprocessor 104 is reduced from 0.6 W to 0.3 W and accordingly, the total of power consumption becomes 1.5 W which is equal to or smaller than the limit of power consumption.

Bus operation time of the image processing circuit 105, the voice processing circuit 106 and the peripheral module 107 operated in high frequency operation mode is respectively 50 %, 5 % and 40 % and bus operation time of the microprocessor 104 operated in middle frequency operation mode is 10 % and accordingly, the total exceeds 105 %. Therefore, the operation mode of the microprocessor 104 having a lower priority of data processing is changed from middle frequency to low frequency, the bus operation time is changed to 5 % and the total of the bus operation time is made to be equal to or smaller than 100 %. The operation mode of the microprocessor 104 becomes low frequency and therefore, power consumption of the microprocessor 104 becomes 0.15 W.

As a result, at time T3, according to operation modes

of respective functional units, the microprocessor 104 is brought into low frequency operation mode, the image processing circuit 105, the voice processing circuit 106 and the peripheral module 107 are brought into high frequency operation mode.

Although according to the embodiment, at time T3, the bus operation time is made to be equal to or smaller than 100 % by changing the microprocessor 104 to low frequency operation mode, the sequence can easily be changed to a control sequence of leaving the microprocessor 104 to middle frequency operation mode and changing the peripheral module 107 having a secondarily low priority from high frequency operation mode to middle frequency operation mode.

In this way, it is possible to control power consumption of the system LSI optimally in a range restrained to be equal to or smaller than the limit of power consumption by determining operation modes of respective functional units from power consumption and bus operation time and priorities of data processings of the respective functional units.

Fig. 5 and Fig. 6 are flowchart diagrams respectively showing control of power consumption and bus of the power-execution control circuit 109. Respective control procedures executed by the clock control circuit 401 and the bus control circuit 402 are shown by the flowcharts.

At first, an explanation will be given of the control procedure of power consumption in reference to Fig. 5.

Step 1: Changes of the operation mode change request signals 444 through 447 from the respective functional units are detected. When the change is detected, the operation proceeds to step 2. When the change is not detected, the operation proceeds to step 1.

Step 2: There is selected power consumption of each functional unit in accordance with its operation mode from power consumption 451a of each functional unit outputted from the power-execution control table 404 (refer to Fig. 3).

Step 3: There is assigned a budget of power consumption to each functional unit in accordance with an order or priority 451c of each functional unit outputted from the power-execution control table 404 from functional units having higher priorities of data processing.

Step 4: It is checked whether a total of the power consumption exceeds the limit of power consumption of LSI. When the total exceeds the limit of power consumption, the operation proceeds to step 5 and when the total does not exceed the limit of power consumption, the operation proceeds to step 6.

Step 5: There is selected an operation mode (clock frequency) so that the power consumption is reduced successively from functional units having lower priorities. Successively, the operation returns to step 4.

Step 6: The bus control circuit 402 is started.

Step 7: End of the operation of the bus control circuit

402 is awaited. When the operation is finished, the operation proceeds to step 8.

Step 8: There is selected a clock frequency in correspondence with the operation mode of each functional unit determined by the bus control circuit 402 and the clock control signals 414 through 417 are outputted. The operation proceeds to step 1.

Successively, an explanation will be given of the control procedure with regard to bus operation time control in reference to Fig. 6.

Step 1: Start of the clock control processing circuit 401 is awaited. When the circuit is started, the operation proceeds to step 2 (step 6 of Fig. 5).

Step 2: There is selected bus operation time of each functional unit in accordance with unit operation mode determined by the clock control processing circuit 401 from individual bus operation time 451b of each functional unit outputted from the power-execution control table 404 (refer to Fig. 3).

Step 3: There is assigned a budget of bus operation time from a priority 451c of each functional unit outputted from the power-execution table 404 from functional units having higher priorities.

Step 4: It is checked wither a total of all bus operation time exceeds 100 %. When the total exceeds 100 %, the operation

proceeds to step 5. When the total does not exceed 100 %, the operation proceeds to step 6.

Step 5: Operation mode is changed so that the bus operation time is reduced successively from functional units having lower priorities. The operation proceeds to step 4.

Step 6: There is outputted the operation mode determined by the bus control circuit 402 to the clock control circuit 401 (step 7 in Fig. 5).

Step 7: The bus operation time is controlled in accordance with the operation mode of each functional unit. In accordance with the bus operation time with regard to the bus request signals 434 through 437 from the respective functional units, bus acknowledge signals (bus operation time control signals) 424 through 427 are outputted to the respective functional units. The operation proceeds to step 1.

In this way, the clock control circuit 401 and the bus control circuit 402 execute simple control and therefore, can be realized in state machine, sequencer and PLA (programmable logic array). Further, these circuits may be controlled by the microprocessor.

Here, Fig. 7 shows a constitution of the bus control circuit 402. The bus control circuit 402 is constituted by a bus control 510 and a bus arbiter 520. The bus control 510 controls the bus operation time in accordance with the flowchart explained in reference to Fig. 6. The bus arbiter 520 receives the bus

operation time 452 for each functional unit assigned by the bus control 510 and outputs the bus acknowledge signals (bus operation time control signals) 424 through 427 to respective functional units in accordance with the bus request signals 434 through 437 from respective functional units so that the bus operation time of each functional unit becomes predetermined time.

A system LSI may be operated to lower (or elevate) power source voltage supplied from outside from a request of a system constituted thereby. This is executed with an object of matching power source voltage with that of a peripheral LSI, an object of lowering power source voltage in order to reduce power consumption or an object of elevating power source voltage in order to heighten an operational frequency. Further, when operated by a dry cell or a storage battery, power source voltage is lowered little by little over time.

When power source voltage is changed in this way, even when a clock frequency is controlled by the power-execution control circuit 109 so that power consumption of LSI becomes equal to or smaller than the limit of power consumption, actual power consumption may differ from a result of calculation. In that case, it is necessary to accurately detect power source voltage supplied to the system LSI and calculate power consumption by using the voltage to thereby execute optimum power control.

Fig. 8 shows a constitution of the voltage detector 110 used in such a case. The voltage detecting circuit 110 inputs the reference voltage Vref from outside and calculates a measured value of power source voltage of the system LSI.

That is, the reference voltage Vref is divided by resistors R1, R2, R3 and R4 and respective divided voltages are designated by notations V1, V2 and V3 and the voltages and the power source voltage VDD are compared by comparators 501 through 503. When an output of the comparator in the case in which the divided voltage is higher than VDD, is set to 0 and an output in the case in which the divided voltage is lower than VDD is set to 1, a point of switching from 0 to 1 becomes the voltage of VDD. The signal is formed into a numerical value (converted into a voltage value) by an encoder 504 and is outputted to the internal bus 10. Thereby, the numerical value is read by the microprocessor 104.

When power consumption P of each functional unit written to the power-execution control table 404 is calculated from power source voltage V, since the power consumption is proportional to square of the voltage and therefore, when actually measured power source voltage becomes Vm, power consumption Pm is calculated by $Pm=PVm^2/V^2$. By rewriting and storing the value of Pm at an area of power consumption for each functional unit of the power-execution control table 404, calculation of power consumption of LSI becomes more accurate.

Further, when the measured value of the power source voltage is intended to measure further accurately, numbers of the voltage dividing resistors and the comparators may be increased.

Further, when the respective functional units are operated by separate voltages, the voltage detectors 110 may be mounted for the respective voltages.

According to the embodiment, in the system LSI mounted with a plurality of functional units, by utilizing for each functional unit the power consumption in accordance with the operation mode (operation clock frequency) as well as the bus operation time necessary for the real time processing and the priority of data processing of each functional unit, the clock frequency and the bus operation time of each functional unit are controlled, thereby, while maintaining the power consumption of the system LSI to be equal to or smaller than the limit of power consumption (upper limit value of power consumption), the real time processing of the functional unit having a higher priority can be realized, thereby, power of the system LSI having high function can be controlled by low power consumption.

(Embodiment 2)

Fig. 9 shows an embodiment in which information of power consumption, individual bus operation time and order of data processing of respective functional units are stored together

to an external memory 500. In Fig. 9, numeral 108 designates an external memory control circuit for reading information stored in the external memory 500 and in initializing, the microprocessor 104 reads information of the external memory 500 by way of the external memory control circuit 108 and writes the information to the power-execution control table 404 at inside of the power-execution control circuit 109. Operation thereafter is similar to that in the case of Embodiment 1.

Further, according to the embodiment, also with regard to the external memory control circuit 108, similar to the other functional units 104 through 107, power and bus operation time can be controlled.

By the embodiment, even after finishing to design LSI, data necessary for controlling power and controlling bus operation time can be supplied from the external memory and therefore, by only rewriting data of the external memory, change of specification of a system can easily be dealt with.

(Embodiment 3)

Fig. 10 shows an embodiment in which information with regard to power consumption, individual bus operation time and priority of data processing of each functional unit are stored by the functional unit per se. In Fig. 10, numerals 204 through 207 designate power-execution memories constituting sub memory means provided respectively to the functional units 104 through 107.

Fig. 11 shows information stored to the power-execution memory 204. The memory circuit 204 constitutes a basis of information stored to the power-execution control table 404 and there are three kinds of high frequency clock mode (200 MHz), middle frequency clock mode (100 MHz) and low frequency clock mode (50 MHz) as operation modes and in each mode, power consumption, individual bus operation time and priority of data processing are stored.

In initializing, the microprocessor 204 respectively reads the information from the memory circuits 204 through 207 and writes the information to the power-execution control table 404 at inside of the power-execution control circuit 109. Operation thereafter is similar to that in the case of Embodiment 1.

By previously providing each functional unit with the information of power consumption, bus operation time and priority in this way, when the system LSI is developed, even in the case in which kinds and a number of pieces of functional units are changed at respective design, various kinds of system LSI can be developed without changing a basic constitution of software applications of the microprocessor 104 for storing power consumption, bus operation time and priority to the power-execution control circuit 109 and the power-execution control circuit 109.

Further, although according to the embodiment, an explanation

has been given such that information with regard to power consumption and bus operation time is stored to the power-execution memories 204 through 207, by writing basic function, basic specification, version information, bug information and the like of the functional unit to the memory circuit of the respective functional unit, even when the system LSI is redesigned by adding or deleting the functional units, by only reading data of the memory circuits, the internal constitution of the system LSI is known and therefore, a control software for controlling the system LSI can correctly be formed (corrected).

As has been described in details, according to the invention, there can be realized the system LSI capable of executing the real time processing by constant power consumption or smaller. Thereby, there can be provided a semiconductor device at a low cost capable of mounting a number of functional units without using a package having a high heat radiating effect or forced cooling.

Further, by previously storing power consumption, bus operation time and priority to the respective functional unit in the system LSI, in initializing, the control software for reading information of these can be made the same and the constitution of the power-execution control circuit can be made the same and power control sequences of various kinds of system LSI can be standardized.

Further, even when the system LSI is used under any operational conditions, the power consumption does not exceed an upper limit value (constant value) and therefore, reliability of a semiconductor device to which the invention is applied and a system adopting the apparatus can be promoted.

Industrial Applicability

The semiconductor device according to the invention can execute a number of kinds of functions, further, the semiconductor device is fabricated at low cost and therefore, applicable widely in the fields of communication, civil apparatus and the like starting from multimedia.

CLAIMS

1. A semiconductor device comprising:

a plurality of functional units connected to each other by an internal bus,

operation mode outputting means provided to each of said plurality of functional units for outputting a request of changing an operation mode at a frequency in operation to other operation mode in accordance with a data processing content, and

power-execution controlling means for controlling a frequency of a clock signal and a bus operation time used by the functional unit executing a processing so that a total of power consumption of the functional unit executing the processing in said plurality of functional units does not exceed a limit of power consumption provided to the semiconductor device in accordance with said request of changing the operation mode.

2. The semiconductor device according to claim 1, wherein said power-execution controlling means comprises;

means for storing information with regard to the power consumption, the individual bus operation time and a priority of data processing for respective operation modes of said plurality of functional units, and

means for assigning the power consumption and the individual bus operation time to the functional block executing

said processing successively from the functional blocks having higher priorities of data processing by using said information, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

3. The semiconductor device according to claim 2,

wherein the means for storing said information comprises a power-execution control table for storing said information, and

wherein the means for supplying said clock control signal and the bus operation time control signal to the functional unit executing said processing comprises a clock control circuit and a bus control circuit respectively generating and outputting said clock control signal and the bus operation time control signal.

4. The semiconductor device according to any one of claims 1 through 3, wherein each of said plurality of functional units includes;

clock selecting means for selecting a clock signal having a corresponding frequency from the plurality of clock signals by receiving said clock control signal, and

data processing means operating with the selected clock signal and setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal.

5. The semiconductor device according to any one of claims 1 through 3, wherein said power-execution controlling means includes means for detecting a change of the operation mode in said request of changing the operation mode and starts an operation of controlling the frequency of the clock signal and the bus operation time at a time point of detecting any change of the operation mode of the functional unit executing the processing.

6. The semiconductor device according to any one of claims 1 through 3, wherein said power-execution controlling means includes means for calculating a total of the power consumption of the functional unit executing the processing and controls to lower the clock frequency of the functional unit having a low priority of data processing so that a total of the calculated power consumption does not exceed the limit of power consumption provided to the semiconductor device.

7. The semiconductor device according to any one of claims 1 through 3, further comprising:

voltage detecting means for detecting a voltage of a power source used internally,

wherein said power-execution controlling means calculates a total of the power consumption of the functional

unit executing said processing by the voltage detected by using said voltage detecting means.

8. The semiconductor device according to claim 1, further comprising:

an external memory for storing the information with regard to the power consumption, the individual bus operation time and the priority of data processing for respective operation modes of said plurality of functional units, and

external memory controlling means for controlling operation of the external memory,

wherein said power-execution controlling means comprises; storing means for storing the information of the external memory read by the external memory controlling means, and

means for assigning the power consumption and the individual bus operation time to the functional block executing said processing successively from the functional blocks having higher priorities of data processing by using the information stored to said storing means, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing

said processing.

9. The semiconductor device according to claim 1,

wherein each of said plurality of functional units includes sub memory means for storing the information with regard to the power consumption, the individual bus operation time and the priority of data processing for respective operation modes, and

wherein said power-execution controlling means includes;

storing means for reading and storing the information stored to the sub memory means, and

means for assigning the power consumption and the individual bus operation time to the functional block executing said processing successively from the functional blocks having higher priorities of data processing by using the information stored to the storing means, setting the frequency of said clock signal in correspondence with the assigned power consumption and setting the assigned individual bus operation time as said bus operation time, and supplying a clock control signal for causing to operate at the set frequency of the clock signal and a bus operation time control signal for causing to use the set bus operation time to the functional unit executing said processing.

10. A semiconductor device comprising:

a plurality of functional units connected to each other by an internal bus, and

a power-execution control circuit for controlling and setting a frequency of a clock signal and a bus operation time used by the functional unit executing a processing so that a total of power consumption of the functional unit executing the processing in said plurality of functional units does not exceed a limit of power consumption provided to the semiconductor device and outputting a clock control signal and a bus operation time control signal for causing the functional unit executing the processing to operate at the set frequency of the clock signal and the set bus operation time,

wherein each of the plurality of functional units includes; a clock selector for selecting the clock signal of a corresponding frequency from the plurality of clock signals by receiving the clock control signal,

a data processing circuit operating with the selected clock signal and setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal,

and

an operation mode output circuit for outputting a request of changing an operation mode at a frequency in operation to other operation mode in accordance with a data processing content, and wherein said power-execution control circuit generates and outputs said clock control signal and said bus operation time control signal in accordance with said request of changing the

operation mode.

11. The semiconductor device according to claim 10, wherein said power-execution control circuit comprises;

a power-execution control table for storing information with regard to the power consumption, the individual bus operation time and priorities of data processing for respective operation modes of said plurality of functional units,

a clock control circuit for assigning the power consumption to the functional block executing said processing successively from the functional blocks having higher priorities of data processing by using said information and outputting said clock control signal by setting the frequency of the clock signal in correspondence with the assigned power consumption, and

a bus control circuit for assigning the individual bus operation time to the functional block executing said processing successively from the functional blocks having the higher priorities of data processing and outputting said bus operation time control signal by setting the assigned individual bus operation time as said bus operation time.

12. The semiconductor device according to claim 10 or 11, wherein said power-execution control circuit starts an operation of outputting said clock control signal and said bus operation time control signal at a time point of outputting a request of changing any operation mode of the functional unit

executing the processing.

13. The semiconductor device according to claim 10 or 11, wherein said power-execution control circuit includes a circuit for calculating a total of the power consumption of the functional unit executing the processing and controls to lower the clock frequency of the functional unit having a lower priority of data processing so that a total of the calculated power consumption does not exceed a limit of power consumption provided to the semiconductor device.

14. The semiconductor device according to claim 10 or 11, further comprising:

a voltage detector for detecting a voltage of a power source used internally,

wherein said power-execution control circuit calculates a total of the power consumption of the functional unit executing said processing by using the voltage detected by the voltage detector.

FIG. 1

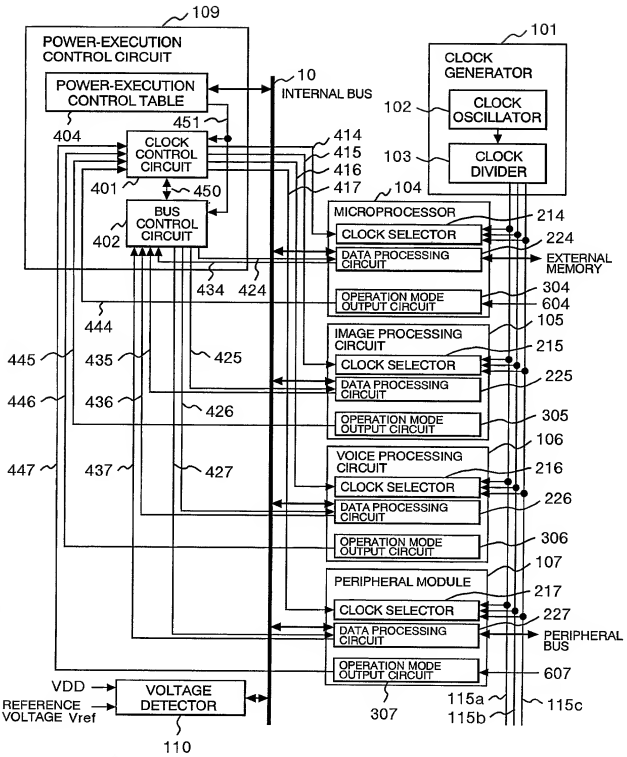
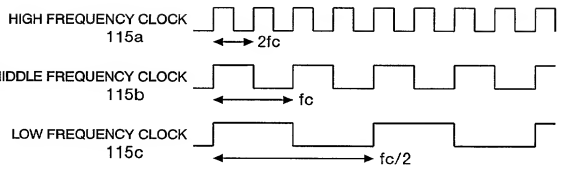

109
POWER-EXECUTION CONTROL CIRCUIT
POWER-EXECUTION CONTROL TABLE
404
451
CLOCK CONTROL CIRCUIT
401
450
BUS CONTROL CIRCUIT
402
10
INTERNAL BUS
414
415
416
417
101
CLOCK GENERATOR
102
CLOCK OSCILLATOR
103
CLOCK DIVIDER
104
MICROPROCESSOR
CLOCK SELECTOR
DATA PROCESSING CIRCUIT
214
224
EXTERNAL MEMORY
OPERATION MODE OUTPUT CIRCUIT
304
604
IMAGE PROCESSING CIRCUIT
105
215
225
305
VOICE PROCESSING CIRCUIT
106
216
226
306
PERIPHERAL MODULE
107
217
227
PERIPHERAL BUS
607
434
424
444
445
435
425
446
436
426
447
437
427
VDD
REFERENCE VOLTAGE Vref
VOLTAGE DETECTOR
110
307
115a
115b
115c

FIG. 2


HIGH FREQUENCY CLOCK
115a
2fc
MIDDLE FREQUENCY CLOCK
115b
fc
LOW FREQUENCY CLOCK
115c
fc/2

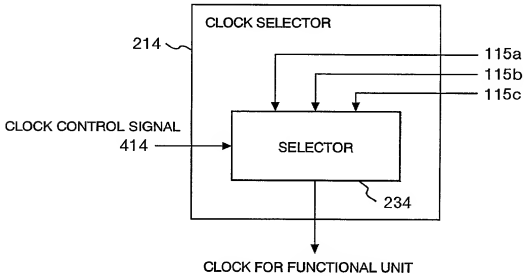

CLOCK SELECTOR
214
115a
115b
115c
CLOCK CONTROL SIGNAL
414
SELECTOR
234
CLOCK FOR FUNCTIONAL UNIT

FIG. 3

		CLOCK		
		200MHz	100MHz	50MHz
POWER CONSUMPTION 451a	MICROPROCESSOR	0.6W	0.3W	0.15W
	IMAGE PROCESSING CIRCUIT	0.6W	0.3W	0.15W
	VOICE PROCESSING CIRCUIT	0.4W	0.2W	0.1W
	PERIPHERAL MODULE	0.2W	0.1W	0.05W
BUS OPERATION TIME 451b	MICROPROCESSOR	20%	10%	5%
	IMAGE PROCESSING CIRCUIT	50%	25%	12%
	VOICE PROCESSING CIRCUIT	5%	5%	5%
	PERIPHERAL MODULE	40%	20%	10%
PRIORITY OF DATA PROCESSING 451c	MICROPROCESSOR	4	7	10
	IMAGE PROCESSING CIRCUIT	2	5	8
	VOICE PROCESSING CIRCUIT	1	1	1
	PERIPHERAL MODULE	3	6	9

404

FIG. 4

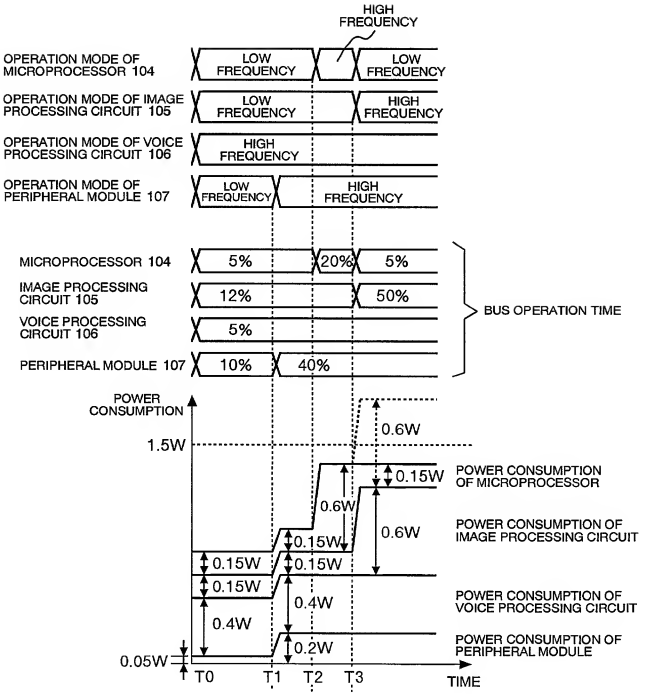

HIGH FREQUENCY
OPERATION MODE OF MICROPROCESSOR 104
LOW FREQUENCY
LOW FREQUENCY
OPERATION MODE OF IMAGE PROCESSING CIRCUIT 105
LOW FREQUENCY
HIGH FREQUENCY
OPERATION MODE OF VOICE PROCESSING CIRCUIT 106
HIGH FREQUENCY
OPERATION MODE OF PERIPHERAL MODULE 107
LOW FREQUENCY
HIGH FREQUENCY
MICROPROCESSOR 104
5%
20%
5%
IMAGE PROCESSING CIRCUIT 105
12%
50%
VOICE PROCESSING CIRCUIT 106
5%
PERIPHERAL MODULE 107
10%
40%
BUS OPERATION TIME
POWER CONSUMPTION
1.5W
0.6W
0.15W
POWER CONSUMPTION OF MICROPROCESSOR
0.6W
0.6W
POWER CONSUMPTION OF IMAGE PROCESSING CIRCUIT
0.15W
0.15W
0.15W
0.15W
0.4W
POWER CONSUMPTION OF VOICE PROCESSING CIRCUIT
0.4W
0.2W
POWER CONSUMPTION OF PERIPHERAL MODULE
0.05W
T0
T1
T2
T3
TIME

FIG. 5

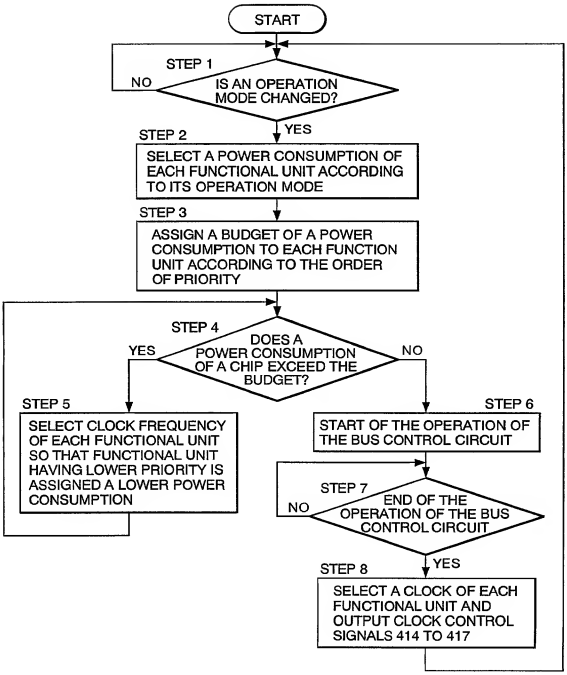

START
STEP 1
IS AN OPERATION MODE CHANGED?
NO
YES
STEP 2
SELECT A POWER CONSUMPTION OF EACH FUNCTIONAL UNIT ACCORDING TO ITS OPERATION MODE
STEP 3
ASSIGN A BUDGET OF A POWER CONSUMPTION TO EACH FUNCTION UNIT ACCORDING TO THE ORDER OF PRIORITY
STEP 4
DOES A POWER CONSUMPTION OF A CHIP EXCEED THE BUDGET?
YES
NO
STEP 5
SELECT CLOCK FREQUENCY OF EACH FUNCTIONAL UNIT SO THAT FUNCTIONAL UNIT HAVING LOWER PRIORITY IS ASSIGNED A LOWER POWER CONSUMPTION
STEP 6
START OF THE OPERATION OF THE BUS CONTROL CIRCUIT
STEP 7
END OF THE OPERATION OF THE BUS CONTROL CIRCUIT
NO
YES
STEP 8
SELECT A CLOCK OF EACH FUNCTIONAL UNIT AND OUTPUT CLOCK CONTROL SIGNALS 414 TO 417

FIG. 6

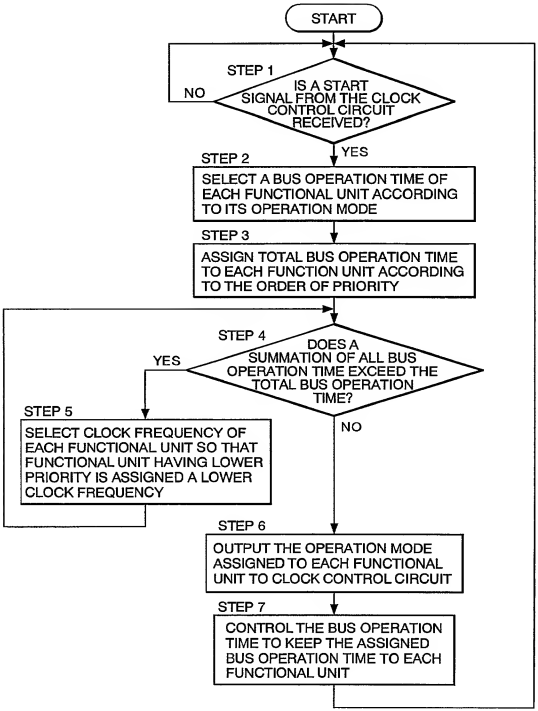

START
STEP 1
IS A START SIGNAL FROM THE CLOCK CONTROL CIRCUIT RECEIVED?
NO
YES
STEP 2
SELECT A BUS OPERATION TIME OF EACH FUNCTIONAL UNIT ACCORDING TO ITS OPERATION MODE
STEP 3
ASSIGN TOTAL BUS OPERATION TIME TO EACH FUNCTION UNIT ACCORDING TO THE ORDER OF PRIORITY
STEP 4
DOES A SUMMATION OF ALL BUS OPERATION TIME EXCEED THE TOTAL BUS OPERATION TIME?
YES
NO
STEP 5
SELECT CLOCK FREQUENCY OF EACH FUNCTIONAL UNIT SO THAT FUNCTIONAL UNIT HAVING LOWER PRIORITY IS ASSIGNED A LOWER CLOCK FREQUENCY
STEP 6
OUTPUT THE OPERATION MODE ASSIGNED TO EACH FUNCTIONAL UNIT TO CLOCK CONTROL CIRCUIT
STEP 7
CONTROL THE BUS OPERATION TIME TO KEEP THE ASSIGNED BUS OPERATION TIME TO EACH FUNCTIONAL UNIT

FIG. 7

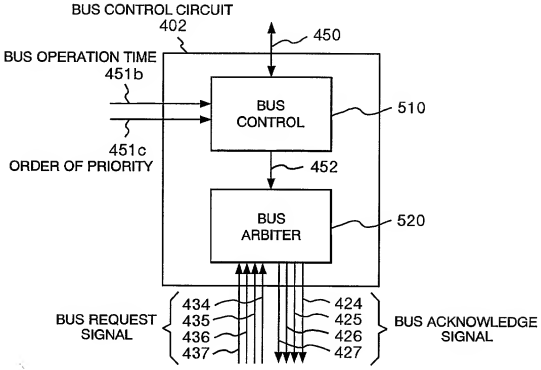

BUS CONTROL CIRCUIT
402
450
BUS OPERATION TIME
451b
BUS CONTROL
510
451c
ORDER OF PRIORITY
452
BUS ARBITER
520
BUS REQUEST SIGNAL
434
435
436
437
424
425
426
427
BUS ACKNOWLEDGE SIGNAL

FIG. 8

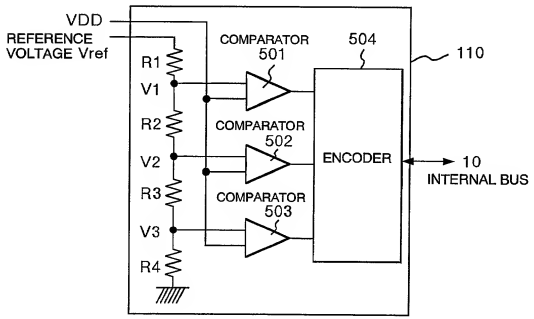

VDD
REFERENCE VOLTAGE Vref
R1
V1
R2
V2
R3
V3
R4
COMPARATOR 501
COMPARATOR 502
COMPARATOR 503
504
110
ENCODER
10
INTERNAL BUS

FIG. 9

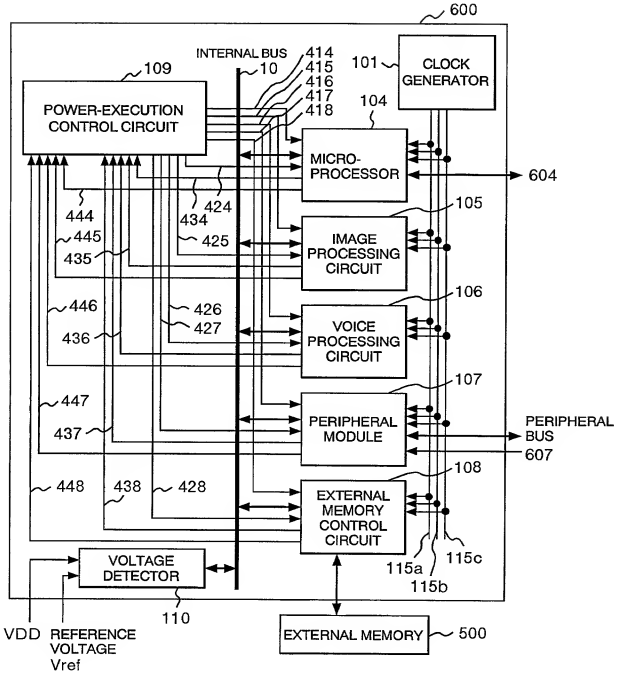

600
INTERNAL BUS
10
414
415
416
417
418
101
CLOCK GENERATOR
109
POWER-EXECUTION CONTROL CIRCUIT
104
MICRO-PROCESSOR
604
105
IMAGE PROCESSING CIRCUIT
106
VOICE PROCESSING CIRCUIT
107
PERIPHERAL MODULE
PERIPHERAL BUS
607
108
EXTERNAL MEMORY CONTROL CIRCUIT
115a
115b
115c
VOLTAGE DETECTOR
110
VDD
REFERENCE VOLTAGE Vref
EXTERNAL MEMORY
500
444
445
435
434
424
425
446
436
426
427
447
437
448
438
428

FIG. 10

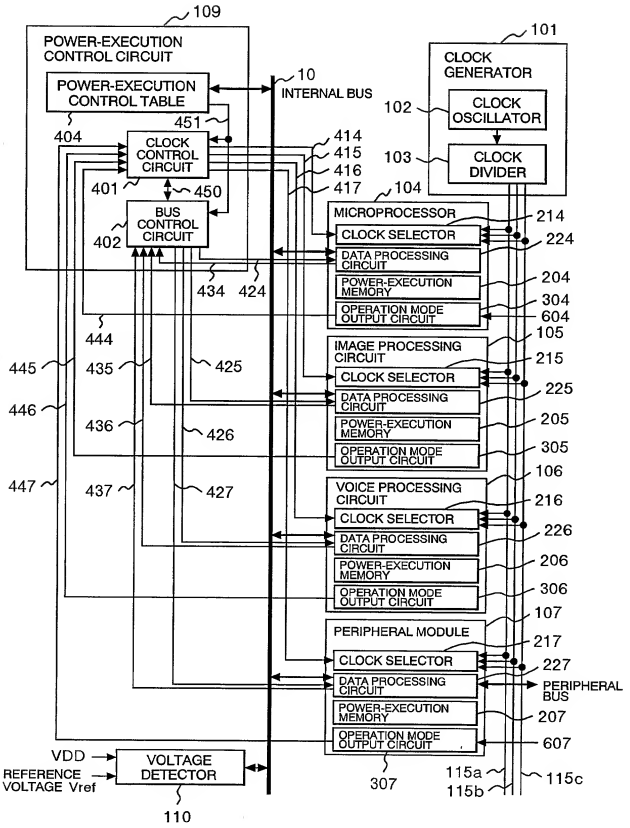

109
POWER-EXECUTION CONTROL CIRCUIT
POWER-EXECUTION CONTROL TABLE
451
404
CLOCK CONTROL CIRCUIT
401
450
BUS CONTROL CIRCUIT
402
10
INTERNAL BUS
414
415
416
417
101
CLOCK GENERATOR
102
CLOCK OSCILLATOR
103
CLOCK DIVIDER
104
MICROPROCESSOR
CLOCK SELECTOR
DATA PROCESSING CIRCUIT
POWER-EXECUTION MEMORY
OPERATION MODE OUTPUT CIRCUIT
214
224
204
304
604
434
424
444
105
IMAGE PROCESSING CIRCUIT
445
435
425
215
225
205
305
446
436
426
106
VOICE PROCESSING CIRCUIT
447
437
427
216
226
206
306
107
PERIPHERAL MODULE
217
227
207
607
PERIPHERAL BUS
VDD
REFERENCE VOLTAGE Vref
VOLTAGE DETECTOR
110
307
115a
115b
115c

FIG. 11

	CLOCK		
	200MHz	100MHz	50MHz
POWER CONSUMPTION	0.6W	0.3W	0.15W
BUS OPERATION TIME	20%	10%	5%
PRIORITY OF DATA PROCESSING	4	7	10

204

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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SYSTEM LSI

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on 29 / June / 1999 as United States Application Number or PCT International Application Number PCT/JP99/03476 and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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(日本語宣言書)

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
			☐
			☐

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I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973 and Carl I. Brundidge, Reg. No. 29,621

書類送付先

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1300 North Seventeenth Street
Arlington, Virginia 22209

直接電話連絡先： (名前及び電話番号)

Direct Telephone Calls to: (*name and telephone number*)

Telephone: (703) 312-6600
Fax: (703) 312-6666

唯一または第一発明者名	Full name of sole or first inventor Takanori SHIMURA
発明者の署名 日付	Inventor's signature Date Takanori Shimura 10/17/2001
住所	Residence Chiba, Japan JPX
国籍	Citizenship Japan
私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

第二共同発明者名		Full name of second joint inventor, if any Keiko KOMATSU
第二共同発明者の署名	日付	Second inventor's signature Date Keiko Komatsu 10/17/2001
住所		Residence Kokubunji, Japan JPX
国籍		Citizenship Japan
私書箱		Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
第三共同発明者名		Full name of third joint inventor, if any
第三共同発明者の署名	日付	Third inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address
第四共同発明者名		Full name of fourth joint inventor, if any
第四共同発明者の署名	日付	Fourth inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address
第五共同発明者名		Full name of fifth joint inventor, if any
第五共同発明者の署名	日付	Fifth inventor's signature Date
住所		Residence
国籍		Citizenship
私書箱		Post Office Address